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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/045,127	10/26/2001	Seungyoon Peter Song	2301P	2410

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EXAMINER	
VITAL, PIERRE M	
ART UNIT	**PAPER NUMBER**
2188	

DATE MAILED: 05/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/045,127	SONG ET AL.	
	Examiner	Art Unit	
	Pierre M. Vital	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-53* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4, 28, 38-53* is/are rejected.

7)☒ Claim(s) *5-27 and 29-37* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 October 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

INFORMATION ON HOW TO EFFECT DRAWING CHANGES

Replacement Drawing Sheets

Drawing changes must be made by presenting replacement figures which incorporate the desired changes and which comply with 37 CFR 1.84. An explanation of the changes made must be presented either in the drawing amendments, or remarks, section of the amendment. Any replacement drawing sheet must be identified in the top margin as "Replacement Sheet" and include all of the figures appearing on the immediate prior version of the sheet, even though only one figure may be amended. The figure or figure number of the amended drawing(s) must not be labeled as "amended." If the changes to the drawing figure(s) are not accepted by the examiner, applicant will be notified of any required corrective action in the next Office action. No further drawing submission will be required, unless applicant is notified.

Identifying indicia, if provided, should include the title of the invention, inventor's name, and application number, or docket number (if any) if an application number has not been assigned to the application. If this information is provided, it must be placed on the front of each sheet and centered within the top margin.

Annotated Drawing Sheets

A marked-up copy of any amended drawing figure, including annotations indicating the changes made, may be submitted or required by the examiner. The annotated drawing sheets must be clearly labeled as "Annotated Marked-up Drawings" and accompany the replacement sheets.

Timing of Corrections

Applicant is required to submit acceptable corrected drawings within the time period set in the Office action. See 37 CFR 1.85(a). Failure to take corrective action within the set period will result in ABANDONMENT of the application.

If corrected drawings are required in a Notice of Allowability (PTOL-37), the new drawings MUST be filed within the THREE MONTH shortened statutory period set for reply in the "Notice of Allowability." Extensions of time may NOT be obtained under the provisions of 37 CFR 1.136 for filing the corrected drawings after the mailing of a Notice of Allowability.

Claim Objections

2. Claims are objected to because of the following informalities:

In claim 53, line 6, it appears that "replacement order generator" should be changed to –and a replacement order generator--.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claim 53 is rejected under 35 U.S.C. 102(e) as being anticipated by Supnet (US6,571,317).

As per claim 53, discloses a method for providing a replacement mechanism in a caching device comprising the steps of: (a) providing at least one replacement order list with N partitions [*4-way set associative*; *LRU data is stored for each set which orders the ways*; col. 5, line 50 – col. 6, line 24]; and (b) arranging the at least one replacement order list with a first to replace position at one end and a last to replace position at an opposite end [*the ways are ordered from most recently used to least recently used*; col. 6, line 15-24; *an entry occupies a position within the order from first to be replaced to last to be replaced*; col. 7, lines 48-64; col. 8, lines 45-52], each position containing a way number [*way0 - way3*; col. 7, lines 1-5], Nway comparators [*comparators 46*; Fig. 2; col. 5, lines 62-63], a control unit [*control circuit 48*; Fig. 2; col. 5, lines 62-63], replacement order generator [*encoding of the value indicates the position of a way within the order*; col. 8, lines 45-52].

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-4, 38-42, 47-48 and 50-52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Supnet (US6,571,317) and Green (US5,970,509).

As per claims 1 and 50, Supnet discloses a caching device using an N-way replacement mechanism comprising: at least one replacement order list with N positions [*4-way set associative*; *LRU data is stored for each set which orders the ways*; col. 5, line 50 – col. 6, line 24], the at least one replacement order list arranged with a first-to-replace position at one end and a last-to-replace position at the opposite end [*the ways are ordered from most recently used to least recently used*; col. 6, line 15-24; *an entry occupies a position within the order from first to be replaced to last to be replaced*; col. 7, lines 48-64; col. 8, lines 45-52], each position containing a way number [*way0 - way3*; col. 7, lines 1-5], N way comparators [*comparators 46*; Fig. 2; col. 5, lines 62-63], a control unit [*control circuit 48*; Fig. 2; col. 5, lines 62-63], a replacement order generator [*encoding of the value indicates the position of a way within the order*; col. 8, lines 45-52].

However, Supnet does not specifically teach receiving a hit signal and, in case of a hit, a hit way number as recited in the claims.

Green discloses receiving a hit signal and, in case of a hit, a hit way number (col. 15, lines 24-27) to provide hit determination circuits able to more rapidly select and

retrieve a data array from a TLB or cache (col. 2, lines 48-50). Since the technology for implementing the receipt of a hit signal and a hit way number in case of a hit was well known and since receiving a hit signal and a hit way number in case of a hit provides hit determination circuits able to more rapidly select and retrieve a data array from a TLB or cache, an artisan would have been motivated to include receiving a hit signal and a hit way number in case of a hit in the system of Supnet. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to use receiving a hit signal and a hit way number in case of a hit, because receiving a hit signal and a hit way number in case of a hit was well known to provide hit determination circuits able to more rapidly select and retrieve a data array from a TLB or cache as taught by Green.

As per claim 2, Supnet does not specifically teach a hit position in the at least one replacement order list is determined by comparing the hit way number with the way number in each of the N positions in the at least one replacement order list using the N way comparators as recited in the claim.

Green discloses a hit position in the at least one replacement order list is determined by comparing a hit way number with a way number in each of N positions in at least one replacement order list using N way comparators [*way 0-3 and way hit 0-3 are sent to MUX 620 using comparator 615 in each of way 0-3*; Fig. 6] to provide hit determination circuits able to more rapidly select and retrieve a data array from a TLB or cache (col. 2, lines 48-50). Since the technology for determining a hit position by comparing a hit way number with the way number using the N way comparators was well known and since

determining a hit position by comparing a hit way number with the way number using the N way comparators provides hit determination circuits able to more rapidly select and retrieve a data array from a TLB or cache, an artisan would have been motivated to include determining a hit position by comparing a hit way number with the way number using the N way comparators in the system of Supnet. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to use determining a hit position by comparing a hit way number with the way number using the N way comparators because it was well known to provide hit determination circuits that are able to more rapidly select and retrieve a data array from a TLB or cache as taught by Green.

As per claim 3, Supnet does not specifically teach the control unit produces replacement order generator control signals using the hit signal and the hit position.

Green discloses a control unit producing replacement order generator control signals using a hit signal and a hit position [col. 15, lines 24-31] to provide a hit determination circuits able to more rapidly select and retrieve a data array from a TLB or cache (col. 2, lines 48-50). Since the technology for implementing producing replacement order generator control signals using a hit signal and a hit position was well known and since producing replacement order generator control signals using a hit signal and a hit position provides hit determination circuits able to more rapidly select and retrieve a data array from a TLB or cache, an artisan would have been motivated to include producing replacement order generator control signals using a hit signal and a

hit position in the system of Supnet. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to use producing replacement order generator control signals using a hit signal and a hit position, because producing replacement order generator control signals using a hit signal and a hit position was well known to provide hit determination circuits able to more rapidly select and retrieve a data array from a TLB or cache as taught by Green.

As per claims 4 and 51, Supnet does not specifically teach the replacement order generator comprises a replace way selector producing a replace way number and N position selectors, each consisting of a multiplexor with at least two inputs as recited in the claim.

Green discloses the replacement order generator comprises a replace way selector producing a replace way number and N position selectors, each consisting of a multiplexor with at least two inputs to improve the rate at which data may be accessed in each of the ways (Fig. 6; col. 15, lines 27-45). Since the technology for implementing a replace way selector consisting of a multiplexor with at least two inputs was well known and since a replace way selector consisting of a multiplexor with at least two inputs improves the rate at which data may be accessed in each of the ways, an artisan would have been motivated to include a replace way selector consisting of a multiplexor with at least two inputs in the system of Supnet. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to use a replace way selector

consisting of a multiplexor with at least two inputs because it was well known to improve the rate at which data may be accessed in each of the ways as taught by Green.

As per claim 38, Supnet does not specifically teach the replacement order generator consists of N position selectors, each selector having the way number from each of the N positions as inputs as recited in the claim.

Green discloses a replacement order generator consisting of N position selectors, each selector having the way number from each of the N positions as inputs [*ways 0-3 are input to MUX 620 using comparator 615 in each of ways 0-3*; Fig. 6] to provide hit determination circuits able to more rapidly select and retrieve a data array from a TLB or cache (col. 2, lines 48-50). Since the technology for determining a selector having the way number from each of the N positions as inputs was well known and since determining a selector having the way number from each of the N positions as inputs provides hit determination circuits able to more rapidly select and retrieve a data array from a TLB or cache, an artisan would have been motivated to include selector having the way number from each of the N positions as inputs in the system of Supnet. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to use determining a selector having the way number from each of the N positions as inputs because it was well known to provide hit determination circuits that are able to more rapidly select and retrieve a data array from a TLB or cache as taught by Green.

As per claims 39 and 52, Supnet discloses a control unit implemented using random access memory or reprogrammable logic array [col. 10, lines 27-34].

As per claim 40, Supnet discloses a caching device as an instruction cache [*instruction cache 12*; Fig. 1].

As per claim 41, Supnet discloses a caching device as a data cache [*data cache 30*; Fig. 1].

As per claim 42, Supnet discloses a caching device as a combined instruction and data cache [col. 7, lines 65-66].

As per claim 47, Supnet discloses a caching device used in a single processor system [Fig. 5; col. 9, lines 54-58].

As per claim 48, Supnet discloses a caching device used in a multiple processor system [Fig. 5; col. 9, lines 54-58].

7. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Supnet (US6,571,317) and Green (US5,970,509) and further in view of Ono (US6,643,737).

As per claim 28, the combination of Supnet and Green discloses the claimed invention as detailed above in the previous paragraphs. However, Supnet and Green do not specifically teach at least one replacement order list has a lock register, indicating the positions in the at least one replacement order list that are locked, and the control unit receiving the value of the lock register as recited in the claim.

Ono discloses a lock mechanism provided in each entry of the ways for improving the utilization efficiency of the cache (col. 5, line 39 – col. 6, line 5). Since the technology for implementing a lock mechanism provided in each entry of the ways was well known and since a lock mechanism provided in each entry of the ways improves the utilization efficiency of the cache, an artisan would have been motivated to implement an instruction TLB in the system of Supnet and Green. Thus, It would have been obvious to one of ordinary skill in the art, at the time the invention to use a lock mechanism provided in each entry of the ways in Supnet and Green, because it was well known to improve the utilization efficiency of the cache as taught by Ono.

8. Claims 43-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Supnet (US6,571,317) and Green (US5,970,509) and further in view of Evans et al. (US6,732,238).

As per claim 43, the combination of Supnet and Green discloses the claimed invention as detailed above in the previous paragraphs. However, Supnet and Green do not specifically teach a caching device as an instruction TLB as recited in the claim.

Evans discloses an instruction TLB provides good performance by speeding processor access to main memory (col. 1, lines 20-23; col. 7, lines 26-28). Since the technology for implementing an instruction TLB was well known and since an instruction TLB provides good performance by speeding processor access to main memory, an artisan would have been motivated to implement an instruction TLB in the system of

Supnet and Green. Thus, It would have been obvious to one of ordinary skill in the art, at the time the invention to use an instruction TLB in Supnet and Green, because it was well known to provide good performance by speeding processor access to main memory as taught by Evans.

As per claim 44, the combination of Supnet and Green discloses the claimed invention as detailed above in the previous paragraphs. However, Supnet and Green do not specifically teach a caching device as a data TLB as recited in the claim.

Evans discloses a data TLB provides good performance by speeding processor access to main memory (col. 1, lines 20-23; col. 7, lines 26-28). Since the technology for implementing a data TLB was well known and since a data TLB provides good performance by speeding processor access to main memory, an artisan would have been motivated to implement a data TLB in the system of Supnet and Green. Thus, It would have been obvious to one of ordinary skill in the art, at the time the invention to use a data TLB in Supnet and Green, because it was well known to provide good performance by speeding processor access to main memory as taught by Evans.

As per claim 45, the combination of Supnet and Green discloses the claimed invention as detailed above in the previous paragraphs. However, Supnet and Green do not specifically teach a caching device as a combined instruction and data TLB as recited in the claim.

Evans discloses a combined instruction and data TLB provides good performance by speeding processor access to main memory (col. 1, lines 20-23; col. 7, lines 26-28). Since the technology for implementing a combined instruction and data TLB was well known and since a combined instruction and data TLB provides good performance by speeding processor access to main memory, an artisan would have been motivated to implement a combined instruction and data TLB in the system of Supnet and Green. Thus, It would have been obvious to one of ordinary skill in the art, at the time the invention to use a combined instruction and data TLB in Supnet and Green, because it was well known to provide good performance by speeding processor access to main memory as taught by Evans.

9. Claim 46 is rejected under 35 U.S.C. 103(a) as being unpatentable over Supnet (US6,571,317) and Green (US5,970,509) and further in view of Wang et al. (US5,831,640).

As per claim 46, the combination of Supnet and Green discloses the claimed invention as detailed above in the previous paragraphs. However, Supnet and Green do not specifically teach a caching device as a texture map cache in a graphics system as recited in the claim.

Wang discloses a texture map cache for increasing the processing efficiency of texture map data requests (col. 3, lines 25-27, 62-65). Since the technology for implementing a texture map cache was well known and since a texture map cache

increases the processing efficiency of texture map data requests, an artisan would have been motivated to implement a texture map cache in the system of Supnet and Green. Thus, It would have been obvious to one of ordinary skill in the art, at the time the invention to use a texture map cache in Supnet and Green, because it was well known to increase the processing efficiency of texture map data requests as taught by Wang.

10. Claim 49 is rejected under 35 U.S.C. 103(a) as being unpatentable over Supnet (US6,571,317) and Green (US5,970,509) and further in view of Aglietti et al (US6,205,519).

As per claim 49, the combination of Supnet and Green discloses the claimed invention as detailed above in the previous paragraphs. However, Supnet and Green do not specifically teach a caching device used in a multithreaded system as recited in the claim.

Aglietti discloses a multithreaded processor used to provide an overall increase in throughput (col. 1, lines 62-64). Since the technology for implementing a multi-threaded processor was well known and since a multi-threaded processor provides an overall increase in throughput, an artisan would have been motivated to implement a multi-threaded processor in the system of Supnet and Green. Thus, It would have been obvious to one of ordinary skill in the art, at the time the invention to use a multi-threaded processor in Supnet and Green, because it was well known to provide an overall increase in throughput as taught by Aglietti.

Allowable Subject Matter

11. Claims 5-27 and 29-37 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

12. The following is a statement of reasons for the indication of allowable subject matter:

(a) As per claim 5, the prior art of record does not teach or suggest "the position selector for the last-to-replace position has the hit way number and the replace way number as inputs and the position selectors for the other positions have its own way number and a replace-later adjacent way number from its adjacent position toward the last-to-replace position as inputs" in combination with the other elements set forth in the claimed invention. Therefore, dependent claims 6-9 are allowable as being dependent upon dependent claim 5 and having additional allowable features therein.

(b) As per claim 10, the prior art of record does not teach or suggest "the at least one replacement order list is divided into one or more partitions with each partition arranged with the first-to-replace position at one end and the last-to-replace position at the opposite end of the partition, and the control unit receiving a reference ID indicating a reference partition" in combination with the other elements set forth in the claimed invention. Therefore, dependent claims 11-27 are allowable as being dependent upon dependent claim 10 and having additional allowable features therein.

(c) As per claim 29, the prior art of record does not teach or suggest "the at least one replacement order list is divided into unlocked and locked partitions, with the unlocked partition arranged with the first-to-replace position at one end and the last-to-replace position at the opposite end of the partition, and the lock register indicating the number of positions in the locked partition" in combination with the other elements set forth in the claimed invention. Therefore, dependent claims 30-37 are allowable as being dependent upon dependent claim 29 and having additional allowable features therein.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is required under 37 C.F.R. § 1.111 (c) to consider these references fully when responding to this action. The documents cited therein teach using an N-way cache replacement, ordering ways for replacement and determining hit position by comparing hit way number with way number.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre M. Vital whose telephone number is (703) 306-5839. The examiner can normally be reached on Mon-Fri, 8:30 am - 6:00 pm, alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (703) 306-2903. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

May 21, 2004

Pierre M. Vital
Examiner
Art Unit 2188